

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S2	94361	(multiplexer)	USPAT	OR	ON	2008/03/24 06:37
S3	7696	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))))	USPAT	OR	ON	2008/03/24 06:41
S4	1100	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1)))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB))	USPAT	OR	ON	2008/03/24 06:42

S5	538	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3)	USPAT	OR	ON	2008/03/24 06:43
S6	229	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3) AND (((direct) adj (memory) adj (access)) or (DMA))	USPAT	OR	ON	2008/03/24 06:44

S7	88	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3) AND ((((direct adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))))	USPAT	OR	ON	2008/03/24 06:46
S8	14	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3) AND ((((direct adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))) AND (((input) or (source) or (channel)) adj ((identifier) or	USPAT	OR	ON	2008/03/24 07:20

		(identification) or (ID)))				
S9	25	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))) AND (((input) or (source) or (channel)) adj2 ((identifier) or (identification) or (ID)))	USPAT	OR	ON	2008/03/24 07:20
S10	13	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3) AND ((((direct) adj (memory) adj	USPAT	OR	ON	2008/03/24 07:21

		(access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))) AND (((input) or (source) or (channel)) adj2 ((identifier) or (identification) or (ID))) AND ((output) adj ((memor\$4) or (FIFO\$1) or (buffer\$1) or (queue\$1) or (register\$1)))				
S11	16	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))) AND (((input) or (source) or (channel)) adj2 ((identifier) or (identification) or (ID))) AND ((output) near2 ((memor\$4) or (FIFO\$1) or (buffer\$1) or (queue\$1) or (register\$1)))	USPAT	OR	ON	2008/03/24 07:24

S12	25	(multiplexer\$1) AND (((multiple) or (plural \$5) or (several)) adj ((input\$1) or (channel \$1))) AND ((memor \$4) or (FIFO\$1) or (buffer\$1) or (queue \$1) or (register\$1)) AND (((multiple) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3) AND ((((direct adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1))) AND (((input) or (source) or (channel)) adj2 ((identifier) or (identification) or (ID)))	USPAT	OR	ON	2008/03/24 07:25
S13	109	(multiplexer\$1) AND (((multiple) or (multi or (plural\$5) or (several)) adj ((input \$1) or (channel\$1))) AND ((memor\$4) or (FIFO\$1) or (buffer\$1) or (queue\$1) or (register\$1)) AND (((multiple) or (multi or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3) AND ((((direct adj (memory) adj (access)) or (DMA))	USPAT	OR	ON	2008/03/24 08:00

		near1 ((controller\$1) or (manager\$1) or (unit\$1)) or (DMAC))				
S14	46	(multiplexer\$1) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((input \$1) or (channel\$1))) AND ((memor\$4) or (FIFO\$1) or (buffer\$1) or (queue\$1) or (register\$1)) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3) AND ((((direct adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1)) or (DMAC)) AND (((input) or (source) or (channel)) near2 ((identifier) or (identification) or (ID)))	USPAT	OR	ON	2008/03/24 08:01
S15	45	(multiplexer\$1) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((input \$1) or (channel\$1))) AND ((memor\$4) or (FIFO\$1) or (buffer\$1) or (queue\$1) or (register\$1)) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit))	USPAT	OR	ON	2008/03/24 08:02

		or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1)) or (DMAC)) AND (((input) or (source) or (channel)) near2 ((identifier) or (identification) or (ID)))AND (((output) or (transmit\$4)) near2 ((memor\$4) or (FIFO\$1) or (buffer\$1) or (queue\$1) or (register\$1)))				
S16	45	(multiplexer\$1) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((input\$1) or (channel\$1))) AND ((memor\$4) or (FIFO\$1) or (buffer\$1) or (queue\$1) or (register\$1)) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((output\$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit\$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1)) or (DMAC)) AND (((input) or (source) or (channel)) near2 ((identifier) or (identification) or (ID)))AND (((output) or (transmit\$4) or (transmission)) near2 ((memor\$4) or (FIFO\$1) or (buffer\$1) or (queue\$1) or (register\$1) or (register\$1)))	USPAT	OR	ON	2008/03/24 08:19

S17	45	\$1))) (multiplexer\$1) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((input \$1) or (channel\$1))) AND ((memor\$4) or (FIFO\$1) or (buffer\$1) or (queue\$1) or (register\$1)) AND (((multiple) or (multi) or (plural\$5) or (several)) adj ((output \$1) or (channel\$1))) AND (((least) adj (significant) adj (bit)) or (LSB)) AND (((most) adj (significant) adj (bit)) or (MSB)) AND (priorit \$3) AND ((((direct) adj (memory) adj (access)) or (DMA)) near1 ((controller\$1) or (manager\$1) or (unit\$1)) or (DMAC)) AND (((input) or (source) or (channel)) near2 ((identifier) or (identification) or (ID)))AND (((output or (transmit\$4) or (transmission)) near2 ((memor\$4) or (FIFO \$1) or (buffer\$1) or (queue\$1) or (register \$1)))	USPAT	OR	ON	2008/03/26 07:00
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